REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claims 1, 7, and 13-16 have been amended. These amendments are necessary and could not have been presented earlier due to the unforeseeability of the arguments presented in the Final Rejection in support of the present rejections.

Claims 1, 5, 6, 13, 15, 20, and 21 were rejected, under 35 USC §102(b), as being anticipated by Lininger (US 3,944,756). Claims 2 and 18 were rejected, under 35 USC §103(a), as being unpatentable over Lininger in view of Kubota et al. (US 5,635,670). Claims 3, 4, and 17 were rejected, under 35 USC §103(a), as being unpatentable over Lininger in view of Takuya (US 4,525,817). Claims 7, 9-12, 14, 16, and 22 were rejected, under 35 USC §103(a), as being unpatentable over Papadopoulos et al. (US 6,504,937) in view of Sondermeyer (US 5,197,102). Claims 8 and 19 were rejected, under 35 USC §103(a), as being unpatentable over Papadopoulos in view of Sondermeyer and further in view of Kubota. Applicant respectfully traverses.

Claim 1 now recites:

> *A condenser microphone apparatus comprising:*
> *a movable electrode which vibrates by an acoustic vibration;*
> *a fixed electrode arranged so as to face said movable electrode;*

a field effect transistor that buffer-amplifies a voltage across said movable electrode and a voltage across said fixed electrode;

a bypass capacitor in which one end is connected to a source terminal, acting as a signal output terminal, of said field effect transistor and the other end is connected to a drain terminal, acting as a common output terminal, of said field effect transistor; and

a series resistor inserted at least in one of an interval between said signal output terminal of said field effect transistor and an output terminal of the apparatus and an interval between said common output terminal of said field effect transistor and a common output terminal of the apparatus.

It is axiomatic that, under 35 USC §102, every limitation of a claim must identically appear in a single prior art reference for it to anticipate the claim. *Gechter v. Davidson, 116 F.3d 1454, 1457, 43 USPQ2d 1030, 1032 (Fed. Cir. 1997).* A finding of anticipation requires that the reference describe all of the elements of the claim, arranged as in the claimed device. *C.R. Bard, Inc. v. M3 Systems, Inc., 157 F.3d 1340, 1349, 48 USPQ2d 1225, 1230 (Fed. Cir. 1998).*

Lininger fails to disclose the feature recited in claim 1 of a bypass capacitor having one end connected to a source terminal, acting as a signal output terminal, of a field effect transistor (FET) and the other end connected to a drain terminal, acting as a common output terminal, of the field effect transistor.

On this point, the Final Rejection proposes that Lininger discloses a bypass capacitor 110, 112 having one end connected to

a signal output terminal of an FET 90 and the other end connected to a common output terminal FET 90 (Final Rejection page 3, third paragraph). Continuing, the Final Rejection proposes that capacitors 110, 112 connect to the "common output (the bottom line, ground) terminal of said field effect transistor (90) (by said pass 108 resistor to the ground and it still connects to the ground (common output)[)]" (page 14, lines 2-6). Although it is unclear from the Final Rejection whether the Office considers Lininger's illustrated circuit ground, FET drain terminal, or both the circuit ground and the FET drain terminal as the structure corresponding to the claimed common output terminal of the FET, the following discussion will elucidate why Lininger does not disclose the structural cooperation between the claimed capacitor and FET.

Lininger discloses in Fig. 3 an FET 90 having exactly three terminals, which are the source, drain, and gate terminals. As discussed in Applicant's Response dated January 15, 2004, two capacitors 110 and 112 are connected between the source terminal (as designated by Lininger in the specification, col. 4, lines 53-61) of FET 90 and a circuit ground. As also mentioned in that Response, a parallel circuit comprising a resistor 108 and a capacitor 114 is connected between the drain terminal of FET 90 and the circuit ground. The gate terminal of FET 90 is connected

to the circuit ground through the series connection of a resistor 128 and a parallel circuit comprising a capacitor 130 and a resistor 126. FET 90 has no other terminals than the source, drain, and gate terminals.

As mentioned above, Lininger's capacitors 110, 112 each have one terminal that connects to the source terminal of FET 90 and another terminal that connects to the circuit ground. Capacitors 110, 112 have only two terminals and neither terminal connects to the drain of FET 90. Although two other capacitors 114, 116 each have a terminal connecting to the drain terminal of FET 90, neither of these two capacitors 114, 116 has a terminal connecting to the source terminal of FET 90.

As apparently stated in the Final Rejection (see page 14, lines 4 and 5), resistor 108 connects to the drain terminal of FET 90 and also connects to the circuit ground. However, this fact does not make the drain terminal of FET 90 equivalent to the circuit ground, as appears to be implied in the Final Rejection, for the operational signals of Lininger's microphone circuit. To presume the drain terminal of FET 90 and the circuit ground are equivalent points for the operation of Lininger's circuit, due to the existence of resistor 108, requires the presumption that resistor 108 is equivalent to a short circuit for all operational signals applied to its terminals.

Applicant has claimed a structure having one terminal of a capacitor connected to the source of an FET and the other terminal connected to the drain of an FET. Lininger's disclosed structure of a capacitor 110, 112 having one terminal connected to the source of FET 90 and the other terminal connected to a first terminal of a resistor 108 and the second terminal of resistor 108 connected to the drain terminal of FET 90 is not identical to the claimed structure, as would be required for anticipation to exist. Lininger's structure is different from the claimed structure and provides a different operational functionality.

Prior to the amendment of the claims contained herein, Applicant did not specifically use the terms "drain" and "source" in claim 1. Instead, the terms "signal output terminal" and "common output terminal" were used.

In Applicant's previous Response, Applicant stated that Lininger did not disclose a capacitor connected between the drain and source terminals of an FET. The Office apparently discounted Applicant's argument, entirely, based on the counter argument that Applicant's claim 1 did not contain a verbatim recitation of "a capacitor connected between the source and drain terminals of the field effect transistor" (see Final Rejection page 14, second paragraph).

Applicant did not describe Lininger's structure using the verbatim nomenclature found in claim 1 because Lininger does not disclose this nomenclature. Instead, Applicant described Lininger's structure using the same terminology employed in Lininger's specification. It was the Office that asserted a correspondence between: (1) the claimed signal output and common output terminals and (2) Lininger's disclosed FET drain and source terminals, not the Applicant. Applicant submits that it is improper for the Office to assert an identity between Lininger's disclosed source and drain terminals and the claimed signal output and common output terminals in its argument for establishing a *prima facie* case of anticipation while at the same time asserting a complete absence of identity between the things identified by the respective sets of nomenclature as used in Applicant's traversal of the *prima facie* case. Accordingly, Applicant respectfully submits that the Office's dismissal of the arguments presented in the previous Response was inappropriate and, as a result, a withdrawal of the finality of the present rejections is warranted.

So as to diminish the potential for further miscommunication due to the nomenclature used in the claims, Applicant has revised claim 1 to recite:

a bypass capacitor in which one end is connected to a source terminal, acting as a signal output terminal, of said field effect transistor and the other end is connected to a drain terminal, acting as a common output terminal, of said field effect transistor.

The signal output terminal of the FET is now specifically identified as the source terminal and the FET's common output terminal is specifically identified as the drain terminal.

Lininger does not disclose a capacitor whose terminals are connected across the drain and source terminals of an FET, regardless of the terminology used to identify components of the claimed structure or Lininger's structure. Because Lininger does not identically disclose the structure defined by claim 1, Lininger cannot anticipate the claimed subject matter. Therefore, allowance of claim 1 and all claims dependent therefrom is warranted.

Independent claims 13 and 15 recite features similar to those distinguishing claim 1 from Lininger. These features distinguish claims 13 and 15 over Lininger for similar reasons that they distinguish claim 1 thereover. Therefore, allowance of claims 13 and 15 and all claims dependent therefrom is warranted.

Independent claim 7 now recites:

A condenser microphone apparatus comprising:
a movable electrode which vibrates by an acoustic vibration;

a fixed electrode arranged so as to face said movable electrode;

amplifying means, comprising a field effect transistor, for buffer-amplifying a voltage across said movable electrode and said fixed electrode, said amplifying means for providing the amplified voltage to a signal output transmission line;

a bypass capacitor in which one end is connected to a source terminal, acting as a signal output terminal, of said field effect transistor and the other end is connected to a drain terminal, acting as a common output terminal, of said field effect transistor, said bypass capacitor operating to bypass a high frequency signal from an external circuit; and

a serial circuit of a blocking capacitor and a damping resistor, in which one end is connected to said signal output terminal of said amplifying means and the other end is connected to the common output terminal of said amplifying means, said serial circuit operating to damp a parallel resonance of an equivalent circuit, comprising said signal output transmission line, said bypass capacitor, and said serial circuit.

The combined teachings of Papadopoulos and Sondermeyer fail to suggest the feature recited in claim 7 of a serial circuit of a blocking capacitor and a damping resistor, in which one end of the serial circuit is connected to a source terminal of an FET and the other end is connected to a drain terminal of the FET. Additionally, the applied references fail to suggest such a serial circuit operating to damp a parallel resonance of an equivalent circuit comprising a signal output transmission line and a bypass capacitor, which is connected across the source and drain terminals of the FET.

The Final Rejection acknowledges that Papadopoulos does not disclose the above-described features of the claimed serial circuit (Final Rejection page 8, third and fourth lines from bottom of page). However, the Final Rejection cites the teachings of Sondermeyer to overcome the deficiencies of Papadopoulos (page 8, last two lines).

As may be seen by inspection of Sondermeyer's drawings, Sondermeyer does not disclose an FET. Therefore, Sondermeyer cannot disclose a bypass capacitor or a series circuit connected across the drain and source terminals of the FET.

Moreover, the serial circuit defined by claim 7 operates to damp a parallel resonance of an equivalent circuit comprising a signal output transmission line and a bypass capacitor. Sondermeyer is silent with regard to the impedance of an output transmission line and the effect this impedance has in conjunction with that of a bypass capacitor. Therefore, Sondermeyer does not suggest an equivalent circuit comprising a signal output transmission line and a bypass capacitor. Because Sondermeyer is silent about these features, it necessarily follows that Sondermeyer cannot suggest damping a parallel resonance of an equivalent circuit comprising the signal output transmission line and bypass capacitor.

By contrast to the claimed structure, Sondermeyer discloses a resonance feedback circuit coupled in parallel with a voltage feedback circuit that reduces the voltage feedback (Sondermeyer abstract). Resonance circuit 60 adjusts the voltage feedback to an amplifier 12 to regulate the damping factor of amplifier 12 and, thereby, modulate the output voltage of amplifier 12 (col. 5, lines 38-43).

Neither Sondermeyer's voltage feedback circuit nor amplifier 12 includes a signal output transmission line as defined by the present invention. Therefore, neither resonance circuit 60, nor any part thereof, damps a parallel resonance of an equivalent circuit comprising the signal output transmission line.

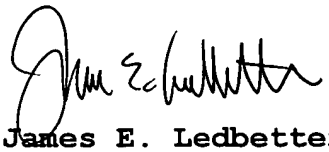
In accordance with the above discussion, Applicant submits that the combined teachings of Papadopoulos and Sondermeyer do not teach or suggest the subject matter defined by claim 7. Therefore, allowance of claim 7 and all claims dependent therefrom is warranted.

Independent claims 14 and 16 recite features similar to those distinguishing claim 7 from Papadopoulos and Sondermeyer. For the same reasons these features distinguish claim 7 over the applied references, so too do they distinguish claims 14 and 16. Therefore, allowance of claims 14 and 16 and all claims dependent therefrom is warranted.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain that may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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